Course : MCA Semester – IV

MICROPROCESSORS, INTERFACING AND APPLICATIONS

Subject Code : 17MCA4C23

1. Intel 8086 is a \_\_\_\_\_\_\_ microprocessor.

**[a] 16-bit** [b] 32-bit [c] 8-bit [d] 64-bit

2. Intel 8086 microprocessor consists of \_\_\_\_\_\_ address lines.

[a] 16 **[b] 20**  [c] 24 [d] 32

3. Which one of the following is a control flag of 8086?

[a] Carry flag [b] Zero flag **[c] Direction flag** [d] Sign flag

4. BIU stands for \_\_\_\_\_\_\_\_\_\_\_\_\_.

[a] Bus Interactive Unit **[b] Bus Interface Unit**  [c] Bus Interrupt Unit

[d] Base Interface Unit

5. EU stands for \_\_\_\_\_\_\_\_\_\_\_\_.

**[a] Execution Unit** [b] Elementary Unit [c] Enable Unit [d] Extended Unit

6. Which one of the following is a segment register?

[a] BP [b] SP **[c] SS** [d] SI

7. The 8086 microprocessor consists of \_\_\_\_\_\_\_ segment registers.

**[a] 4** [b] 3 [c] 2 [d] 8

8. DS is referred to as \_\_\_\_\_\_ register.

[a] Decode Segment [b] Divide Segment [c] Digital Segment **[d] Data Segment**

9. DI is a \_\_\_\_\_\_\_\_\_ register.

[a] pointer **[b] index** [c] data [d] base

10. The Instruction Pointer is \_\_\_\_\_\_ in length.

**[a] 16 bits** [b] 20 bits [c] 8 bits [d] 12 bits

11. The size of a memory segment of 8086 is \_\_\_\_\_\_.

[a] 64 MB [b] 2 MB [c] 1 MB **[d] 64 KB**

12. The 8086 fetches instructions from the \_\_\_\_\_\_\_ segment of the memory.

[a] stack **[b] code** [c] extra [d] data

13. The 8088 microprocessor consists of a \_\_\_\_\_\_\_\_\_ instruction queue.

[a] 6-byte **[b] 4-byte** [c] 3-byte [d] 5-byte

14. The functions of pins \_\_\_\_\_\_\_ depend on the mode in which 8086 is operating.

**[a] 24-31** [b] 22-29 [c] 14-21 [d] 16-23

15. If MN/MX is low, the 8086 microprocessor operates in \_\_\_\_\_\_\_\_ mode.

[a] intermediate **[b] minimum** [c] maximum [d] min-max

16. The 8086 microprocessor supports \_\_\_\_\_\_ types of instruction formats.

**[a] 6** [b] 4 [c] 8 [d] 12

17. The 8088 microprocessor consists of a \_\_\_\_\_\_\_\_\_ data lines.

[a] 16 [b] 20 **[c] 8** [d] 12

18. DEN stands for \_\_\_\_\_\_\_\_\_.

[a] Direct Enable [b] Direct Encode [c] Data Encode **[d] Data Enable**

19. MOV AX, BX is an example of \_\_\_\_\_\_\_\_\_\_\_ addressing instruction.

[a] direct [b] indirect [c] immediate  **[d] register**

20. Which one of the following registers is used in I/O addressing?

**[a] DX**  [b] AX [c] CX [d] BX

21. The \_\_\_\_\_\_\_\_\_ is a set of conductors that connects the CPU to its memory and I/O devices.

**[a] system bus** [b] I/O bus [c] memory bus [d] data bus

22. The addressing capacity of Intel 8086 microprocessor is \_\_\_\_\_\_\_\_\_\_.

[a] 64 MB [b] 2 MB **[c] 1 MB** [d] 64 KB

23. The current status of the processor is stored in a register called \_\_\_\_\_\_\_\_\_\_.

[a] program status word [b] instruction register

[c] status register  **[d] processor status word**

24. Intel 8086 microprocessor consists of \_\_\_\_\_\_ conditional flags and \_\_\_\_\_\_ control flags.

**[a] 6, 3** [b] 4, 5 [c] 3, 6 [d] 5, 4

25. In register indirect addressing the effective address of the operand is in the \_\_\_\_\_ register.

[a] DX [b] AX [c] CX **[d] BX**

26. The correct assembler instruction format of 8086 is:

**[a] Label : Mnemonic Operand, Operand ; Comments**

[b] Mnemonic Operand, Operand : Comments ; Label

[c] Comments; Label : Mnemonic Operand, Operand

[d] Mnemonic Operand, Operand : Label ; Comments

27. The instruction LEA stands for \_\_\_\_\_\_\_\_\_\_\_.

[a] Label Effective Address **[b] Load Effective Address**

[c] Load Extended Address [d] Label Extended Address

28. For a MOV DST, SRC instruction, the destination cannot be \_\_\_\_\_\_\_\_.

[a] memory [b] register **[c] immediate**  [d] direct

29. The CWD instruction extends the sign of the word in \_\_\_\_\_ to DX thus forming a double word.

[a] DX **[b] AX**  [c] CX [d] BX

30. The \_\_\_\_\_\_\_ instruction finds the 2’s complement of an operand.

[a] XOR [b] CMP [c] NOT **[d] NEG**

31. The MUL BL instruction multiplies the content of \_\_\_\_\_ by the content of BL.

[a] AX **[b] AL**  [c] CL [d] BX

32. The DIV CL instruction places the remainder in \_\_\_\_\_\_\_ register.

[a] AX [b] AL **[c] AH**  [d] CL

33. The instruction DAA stands for \_\_\_\_\_\_\_\_\_\_\_.

**[a] Decimal Adjust for Addition** [b] Data Adjust for Addition

[c] Decimal Adjust for Accumulator [d] Data Adjust for Accumulator

34. The instruction JP OPR means \_\_\_\_\_\_.

[a] Branch if not Positive [b] Branch if Parity Odd

[c] Branch if Positive **[d] Branch if Parity Even**

35. The LOOP OPR instruction \_\_\_\_\_\_\_\_\_\_.

**[a] checks the CX register** [b] checks the BX register

[c] checks the AX register [d] checks the DX register

36. The CLC instruction \_\_\_\_\_\_\_\_\_\_.

[a] clears CX register **[b] clears carry flag**

[c] clears CL register [d] clears CH register

37. The CMC instruction \_\_\_\_\_\_\_\_\_\_.

[a] complements CX register [b] compares carry flag

**[c] complements carry flag** [d] complements CL register

38. The STD instruction \_\_\_\_\_\_\_\_\_\_.

[a] stores data into a register [b] sets data into register

[c] store temporary data **[d] sets the direction flag**

39. The CLI instruction \_\_\_\_\_\_\_\_\_\_.

[a] Clear Logical Instruction **[b] Clears Interrupt flag**

[c] Clear Instruction [d] Compare Logical Instruction

40. The STC instruction \_\_\_\_\_\_\_\_\_\_.

**[a] Sets Carry flag** [b] Store Carry flag

[c] Store Tag for Carry [d] Set Time Clock

41. The NOT OPR instruction \_\_\_\_\_\_\_\_\_\_.

[a] finds 2’s complement of OPR [b] clears the content of OPR

**[c] finds 1’s complement of OPR** [d] complements output register OPR

42. Which one of the following operations is performed during TEST instruction?

[a] OR **[b] AND** [c] XOR [d] NOT

43. In the instruction SHR OPR, CNT the destination OPR can have any of the 8086 addressing modes except the \_\_\_\_\_\_\_\_\_ mode.

**[a] immediate**  [b] indirect [c] implied [d] direct

44. In the instruction ROL OPR, CNT, the value of CNT must be 1 or \_\_\_\_\_\_\_\_.

[a] CX [b] CH **[c] CL** [d] 0

45. Which one of the following registers is true with RCL instruction?

[a] Reverse Carry Left [b] Rotate CL register

[c] Rotate Carry Left **[d] Rotate left through carry**

46. The instruction MOVSB \_\_\_\_\_\_\_\_\_.

**[a] moves byte string**  [b] moves bit string [c] Moves BX [d] Moves BL

47. Which one of the following instructions affects condition flags?

[a] LODSB [b] STOSB **[c] SCASB** [d] LODSW

48. The REP Prefix repeatedly executes the specified string instruction until \_\_\_\_.

**[a] CX = 0**  [b] CH = 0 [c] CL **= 0** [d] CF = 0

49. Which one of the following instructions is correct?

[a] ADC AX, AL [b] ADC AH, AX **[c] ADC AX, BX** [d] ADC BX

50. The LODSB instruction loads the content of content of SI into \_\_\_\_\_\_ register.

[a] AX **[b] AL** [c] AH [d] BL

51. When different lines are used for the two signal directions the communication system is said to be \_\_\_\_\_\_\_\_.

**[a] full duplex** [b] half duplex [c] simplex [d] simple duplex

52. \_\_\_\_\_\_\_ uses the same line for both input and output but not simultaneously.

[a] full duplex **[b] half duplex** [c] simplex [d] simple duplex

53. The first bit of an asynchronous character format is always 0 and is called the \_\_\_\_\_\_\_.

[a] stop bit [b] mark bit **[c] start bit** [d] end bit

54. The last bits of an asynchronous character format are 1s and are called \_\_\_\_\_\_\_.

**[a] stop bits** [b] mark bits [c] start bits [d] parity bits

55. When a 0 is seen instead of a stop bit a \_\_\_\_\_\_ error is said to occur.

**[a] framing** [b] parity [c] overrun [d] underrun

56. UART stands for \_\_\_\_\_\_\_\_\_\_\_.

[a] Uniform Asynchronous Remote Transmitter

[b] Universal Asynchronous Remote Transmitter

**[c] Universal Asynchronous Receiver Transmitter**

[d] Universal Asynchronous Remote Transfer

57. If a character is not available at the beginning of an interval, an \_\_\_\_ error is said to occur.

[a] framing [b] parity [c] overrun **[d] underrun**

58. Which one of the following is a programmable communication interface?

[a] 8255 [b] 8237 [c] 8259 **[d] 8251**

59. DSR stand for\_\_\_\_\_\_\_\_.

[a] Direct Set Ready **[b] Data Set Ready** [c] Data Sync Ready [d] Dynamic Sync Ready

60. CTS is a \_\_\_\_\_\_\_\_\_\_\_ signal

**[a] Clear to Send** [b] Control Transmitter

[c] Connect to Send [d] Control Tansfer Sync

61. In the asynchronous mode register of 8251, PEN is \_\_\_\_\_\_\_\_ signal.

[a] Process empty [b] Program enable [c] Process enable **[d] Parity enable**

62. In the synchronous mode register of 8251, ESD is \_\_\_\_\_\_\_\_ signal.

[a] Error System Detect **[b] External Synchronous Detect**

[c] Error Status Detect [d] External Status Detect

63. In the control register of 8251, SBRK causes a break by forcing \_\_\_\_\_ low.

[a] RxD **[b] TxD** [c] TxRDY [d] RxRDY

64. The TxE signal indicates that the transmitter is \_\_\_\_\_\_\_\_.

**[a] empty** [b] enabled [c] receiving data [d] sending data

65. PPI stands for \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

[a] Programmable Peripheral Interrupt

**[b] Programmable Peripheral Interface**

[c] Programmable Processor Interface

[d] Peripheral Processor Interface

66. Intel 8255 is a \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

[a] DMA controller **[b] PPI** [c] CRT controller [d] floppy disk controller

67. \_\_\_\_\_\_\_ can be operated in mode 2.

[a] Port B [b] Port C(upper) **[c] Port A** [d] Port C(lower)

68. Intel 8255 consists of \_\_\_\_\_\_\_ 8-bit ports.

[a] 8 [b] 2 [c] 4 **[d] 3**

69. Which of the following ports are available in Mode 1?

[a] All the ports [b] Port A and Port C [c] Port B and Port C  **[d] Port A and Port B**

70. In Mode 1 and Mode 2, \_\_\_\_\_\_\_\_\_ acts as the control signals.

**[a] Port C**  [b] Port A [c] Port B [d] data bus

71. DMA stands for \_\_\_\_\_\_\_\_\_\_.

**[a] Direct Memory Access** [b] Data Memory Access

[c] Data Mapped Access [d] Direct Mapped Access

72. Which one of the following is a programmable peripheral interface?

**[a] 8255** [b] 8237 [c] 8259 [d] 8251

73. Which one of the following is a DMA controller?

[a] 8255 **[b] 8237** [c] 8259 [d] 8251

74. The signal EOP stands for \_\_\_\_\_\_\_\_\_.

[a] End of Program [b] Enable Output **[c] End of Process** [d] Enable Output Process

75. Mode-1 of 8255 is the \_\_\_\_\_\_\_\_\_\_ mode of operation.

[a] simple input/output [b] bidirectional **[c] strobed input/output** [d] direct

76. A delay subroutine should end with a \_\_\_\_\_\_\_ instruction.

[a] CALL [b] HLT **[c] RET** [d] EI

77. The time for one state in Intel 8085 is \_\_\_\_\_\_\_\_.

[a] 350 ms [b] 350 ns [c] 320 ms **[d] 320 ns**

78. LED stands for \_\_\_\_\_\_\_\_\_\_\_\_\_.

[a] Light Emitting Device **[b] Light Emitting Diode**

[c] Light Effective Device [d] Light Excitation Diode

79. In a common-cathode 7-segment display the number \_\_\_\_\_ is displayed by applying logic ‘1’ to the segments *a, b, d, e,* and *g*.

[a] 5 [b] 6 [c] 8 **[d] 2**

80. \_\_\_\_\_\_\_\_\_ is an example of a common-cathode 7-segment display.

**[a] FND 500** [b] FND 507 [c] FND 510 [d] MAN 72

81. \_\_\_\_\_\_\_\_\_ is an example of a common-anode 7-segment display.

[a] FND 500 **[b] FND 507**  [c] FND 503 [d] MAN 74

82. In a common-cathode type display, all the cathodes of LEDs are tied together to \_\_\_\_\_\_.

[a] +5V **[b] ground**  [c] the anode [d] the segments

83. In a common-anode type display, all the anodes of LEDs are tied together and connected

to \_\_\_\_\_\_.

**[a] +5V** [b] ground [c] the anode [d] the segments

84. In a frequency measurement system, the point at which the square wave changes from 0 to 1 is called \_\_\_\_\_\_\_ point.

[a] one instant [b] changeover **[c] zero instant** [d] conversion

85. The instruction CMP B \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

**[a] compares A and B registers** [b] complements B register

c] compares B and C registers [d] complements BC pair

86. A \_\_\_\_\_\_\_ is used to get a voltage proportional to temperature.

[a] transistor **[b] thermocouple**  [c] capacitor [d] resister

87. In a temperature measurement system, the microprocessor sends a \_\_\_\_\_\_\_ signal to A/D converter.

[a] ready [b] control **[c] start of conversion** [d] end of conversion

88. In a temperature measurement system, the A/D sends a \_\_\_\_\_\_\_ signal to the Microprocessor.

[a] ready [b] control [c] start of conversion **[d] end of conversion**

89. On receiving the E/C signal the microprocessor reads the output of the \_\_\_\_\_\_\_.

[a] display device [b] D/A converter **[c] A/D converter** [d] thermocouple

90. The instruction \_\_\_\_\_\_\_ increments the content of HL pair.

**[a] INX H** [b] INR H [c] INR M [d] INR HL

91. Which of the following instruction is used to invoke a subroutine in the main program?

**[a] CALL** [b] RET [c] SUB [d] JMP

92. The instruction IN 03 transfers \_\_\_\_\_\_\_\_.

[a] the data 03 into the accumulator [b] content of port 03 into the memory

**[c] content of port 03 into accumulator** [d] data 03 into memory

93. In a water level indicator, when a probe is immersed in water, it is at \_\_\_\_\_\_\_\_.

[a] +5V potential [b] high potential [c] positive **[d] ground potential**

94. In a water level indicator, when a probe is not immersed in water, it is at \_\_\_\_\_\_\_\_.

**[a] +5V potential** [b] high potential [c] positive [d] ground potential

95. In a water level indicator, the probes are connected to the 8255 through \_\_\_\_\_\_\_\_.

[a] converter [b] buffer **[c] inverter** [d] ADC

96. Which of the following instruction rotates the content of accumulator towards left including carry?

[a] RLC [b] RRC [c] RAR **[d] RAL**

97. The JC NEXT instruction jumps to the address NEXT if the \_\_\_\_\_ flag is set.

[a]auxiliary carry [b] parity [c] sign  **[d] carry**

98. In a microprocessor-based traffic control system, all the ports of 8255 are programmed as \_\_\_\_\_\_\_\_\_\_ ports.

[a] input **[b] output** [c] input and output [d] control

99. In a microprocessor-based traffic control system, all the ports of 8255 are programmed to operate in \_\_\_\_\_\_\_.

[a] Mode 1 [b] Mode 2 **[c] Mode 0** [d] Mode 1 and 2

100. The control word to make all ports as output ports in mode 0 operation is \_\_\_\_\_\_\_.

**[a] 80H** [b] 98H [c] 88H [d] 89H